REMARKS/ARGUMENTS

After the foregoing Amendment, Claims 1-19 are currently pending in this application. Claims 1, 2, 5, 6, and 16-19 have been amended to more distinctly claim subject matter which the Applicants regard as the invention. Applicants submit that no new matter has been introduced into the application by these amendments.

Allowable Subject Matter

The Examiner is thanked for indicating that claims 3, 4, 7, and 8 contain allowable subject matter, and that claims 9-15 are allowed.

Claim Rejections - 35 USC § 102(b)

Claims 1, 2, 5, 6, and 16-19 stand rejected under 35 USC § 102(b) as being allegedly anticipated by Saxena (U.S. Patent No. 5,734,664, hereinafter "*Saxena*"). Applicants respectfully traverse this rejection.

The present claims are directed to writing data to and reading data from a plurality of memory devices of the same width in a memory system. In an exemplary embodiment, a code word having a plurality of bits is partitioned into groups of bits called nibbles, each nibble having a width equal to the width of the memory devices. The width of the nibbles and the memory devices can be any number of bits. Groups of adjacent nibbles are stored on each memory device in corresponding address lines. The code word can comprise a data block and error detection and correction bits generated for the data block. If so, if one of the memory devices fails or if data contained in a memory device is errant, the error detection and correction bits can be used to recover the missing or errant data. In an embodiment, the memory system

comprises 36 memory devices, each having a width of 4 bits, the code word comprises 288 bits, the code word is partitioned into 72 sequentially numbered nibbles of 4 bits each, and pairs of adjacent even and odd numbered nibbles are stored in the memory devices, each device storing a different pair of nibbles, the even and odd nibbles being stored in respective address lines of the memory devices.

It is well settled that a reference must teach every element or aspect of a claim in order to be considered prior art under 35 USC § 102(b).

In contrast to the claimed invention, *Saxena* discloses using a plurality of memory devices in a memory system, wherein, "rather than store data in groups of bits equal to the width of the memory chip, data is stored in groups of bits smaller than the width of a chip.... Because the group is smaller than the width of the chip, a smaller error code may be used." (*Saxena*, Abstract). This is easily distinguishable from the present claims, wherein the nibbles (i.e., groups of bits) and the memory devices have the same width.

In particular, in an embodiment in *Saxena*, "sixteen eight bit wide, 4 megabit addressable memory devices ... are each used to hold two four bit wide nibbles in each half". (*Saxena* column 4 lines 5-10). In *Saxena*, nibbles must have a smaller width than the memory devices in which they are stored. This is because *Saxena* effectively divides the memory devices into fields having a width smaller than the devices. *Saxena* is motivated to do this because the error codes operable on the smaller width fields are more compact than the error codes operable directly on the larger width devices. Because the error codes are more compact, they require less storage, so more of the memory devices' capacity can be used to store data instead of error codes. "Thus, the number of check bits is smaller for the same size data stored in devices having smaller widths. The problem of larger numbers of check bits required for larger memory devices is

exacerbated by the fact that larger numbers of check bits may not fit in the device exactly, which can require additional storage space." (*Saxena*, column 3, lines 11-16). The solution to this problem taught by *Saxena* is to divide the width of the memory devices into smaller width fields, such as two fields each of half the width of the devices, in effect treating the memory devices as pairs of " addressable memory devices with widths smaller than the actual memory devices [which] allows the use of more compact error codes." (*Saxena* column 6 lines 53-55).

The approach recited in the present claims is incompatible with *Saxena*. In *Saxena*, the width of nibbles is smaller than the width of the memory devices, the memory devices are divided into smaller fields equal to the width of the nibbles, and the nibbles are stored in those smaller fields. Thus, for example, if the memory system of *Saxena* were used to store a data block such as a code word having a width much larger than the width of a memory device, only a single nibble of the data block, a fraction of the width of a memory device, would be stored in each memory device. In dramatic contrast, the present claims recite partitioning a code word into a plurality of nibbles each having a width equal to the width of the memory devices, grouping the nibbles into groups of adjacent nibbles, and storing each group in a different memory device. Thus, in *Saxena* each memory device stores only a single nibble of a data block, and the nibble's width is a fraction of the width of the memory device. In contrast, in the present claims each memory device stores a plurality of nibbles, and each nibble's width is equal to that of the memory device.

Even if, for the sake of argument, *Saxena* did teach storing more than one nibble from the same data block in each memory device (which it does not), *Saxena* does not teach storing successive nibbles of the data block into a plurality of corresponding address lines in each of the memory devices, as do the present claims.

Because *Saxena* does not teach all of the elements of independent claims 1, 5, and 16-19, *Saxena* does not anticipate those claims under 35 USC § 102(b), and they are allowable over *Saxena*. Claim 2 depends from claim 1, and claim 6 depends from claim 5. Therefore, without prejudice to their individual merits, claims 2 and 6 are also allowable.

Based on the arguments presented above, withdrawal of the 35 USC § 102(b) rejection of claims 1, 2, 5, 6, and 16-19 is respectfully requested.

Conclusion

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1 - 19, is in condition for allowance and a notice of allowance is respectfully requested.

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

Respectfully submitted,

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